REMARKS

In the Office Action, the Examiner rejects claims 13 and 14 under 35 U.S.C. § 102(e) as anticipated by WU et al. (U.S. Patent Application Publication No. 2004/0048424); and rejects claims 1-12 and 15-19 under 35 U.S.C. § 103(a) as unpatentable over WU et al. in view of FRENETTE et al. (U.S. Patent No. 5,770,490). Applicants respectfully traverse these rejections.

By way of the present amendment, claim 20 has been added. No new matter has been added by way of the present amendment. Claims 1-20 are pending.

Claims 13 and 14 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by WU et al. Applicants respectfully traverse.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. WU et al. does not disclose or suggest the combination of features recited in claims 13 and 14.

For example, independent claim 13 is directed to a method for doping fin structures in FinFET devices. The method includes forming a first glass layer on the fin structures of a first area and a second area; removing the first glass layer from the second area; forming a second glass layer on the fin structures of the first area and the second area; and annealing the first area and the second area to dope the fin structures of the first area and the second area. WU et al. does not disclose or suggest this combination of features.

For example, WU et al. does not disclose or suggest annealing the first area and the second area to dope the fin structures of the first area and the second area. The Examiner relies on Fig. 9B and para. 0023 of WU et al. for allegedly disclosing this feature (Office Action, pg. 2). Applicants disagree.

Fig. 9B of WU et al. depicts a cross-sectional view of a FINFET device where the portion of the FINFET under PSG layer 12 is an N type source/drain region 40 and the portion of the FINFET under BSG layer 10 is a P type source/drain region 30. This figure of WU et al. in no way discloses or suggests annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13. Contrary to the Examiner's position, Fig. 9B of WU et al. does not disclose fin structures, but merely an N type source/drain region 40 and a P type source/drain region 30. As will be appreciated by one skilled in the art, a fin structure for a FINFET device is positioned between the source and drain regions of the FINFET device. Therefore, as illustrated in WU et al.'s Fig. 9A, the fin structures of WU et al.'s FINFET device are positioned below gate structure 8. WU et al. does not disclose or suggest annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13.

At para. 0023, WU et al. discloses:

> An anneal procedure is next performed at a temperature between about 700 to 1000 °C, for a time between about 1 to 60 min, in a conventional furnace, or via use of rapid thermal anneal (RTA) procedures. The anneal procedure allows the doping of the exposed SOI shapes which directly underlay the doped insulator layer, resulting in doped source/drain regions. The portion of FINFET shape 5, underlying PSG layer 12, is now N type source/drain region 40, while the portions of FINFET shape 6, underlying BSG layer 10, is now P type source/drain region 30. This is

> schematically shown in cross-sectional style in FIG. 9B, and as a top view using FIG. 9A. Therefore a desired NMOS FINFET device, featuring N type source/drain region 40, and a desired PMOS FINFET device, featuring P type source/drain region 30, is defined in the same SOI layer.

This section of WU et al. discloses annealing the FINFET device to dope the source and drain regions. This section of WU et al. in no way discloses or suggests annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13. Instead, as set forth above, WU et al. merely discloses the doping of source and drain regions.

The Examiner has not pointed to any section of WU et al. that discloses or suggests annealing the first area and the second area to dope the fin structures of the first area and the second area, as required by claim 13.

Since WU et al. does not disclose every feature of Applicants' claim 13, WU et al. cannot anticipate claim 13.

For at least the foregoing reasons, Applicants submit that claim 13 is not anticipated by WU et al.

Claim 14 depends from claim 13. Therefore, this claim is not anticipated by WU et al. for at least the reasons given above with respect to claim 13.

Claims 1-12 and 15-19 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over WU et al. in view of FRENETTE et al. Applicants respectfully traverse.

Independent claim 1 is directed to a method for forming FinFET devices. The method includes forming a first fin structure, a source region, and a drain region in a first area of a wafer; forming a second fin structure, a source region, and a drain region in a

second area of the wafer; forming a phosphosilicate glass layer on the first area and the second area; removing the phosphosilicate glass layer from the second area; forming a boron silicate glass layer on the first area and the second area; annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron; removing the boron silicate glass layer from the first area and the second area; and removing the phosphosilicate glass layer from the first area. WU et al. and FRENETTE et al. do not disclose or suggest this combination of features.

For example, WU et al. and FRENETTE et al. do not disclose or suggest annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron. The Examiner relies on Fig. 9B and para. 0023 of WU et al. for allegedly disclosing this feature (Office Action, pp. 3-4). Applicants disagree.

As set forth above, Fig. 9B of WU et al. depicts a cross-sectional view of a FINFET device where the portion of the FINFET under PSG layer 12 is an N type source/drain region 40 and the portion of the FINFET under BSG layer 10 is a P type source/drain region 30. This figure of WU et al. in no way discloses or suggests annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to

be doped with boron, as required by claim 1. Contrary to the Examiner's position, Fig. 9B of WU et al. does not disclose fin structures, but merely an N type source/drain region 40 and a P type source/drain region 30. As will be appreciated by one skilled in the art, a fin structure for a FINFET device is positioned between the source and drain regions of the FINFET device. Therefore, as illustrated in WU et al.'s Fig. 9A, the fin structures of WU et al.'s FINFET device are positioned below gate structure 8. WU et al. does not disclose or suggest annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1.

Para. 0023 of WU et al. is reproduced above. This section of WU et al. discloses annealing the FINFET device to dope the source and drain regions. This section of WU et al. in no way discloses or suggests annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1. Instead, as set forth above, WU et al. merely discloses the doping of source and drain regions. The disclosure of FRENETTE et al. does not remedy this deficiency in the disclosure of WU et al.

The Examiner has not pointed to any section of WU et al. or FRENETTE et al. that discloses or suggests annealing the first area and the second area, where the annealing causes the first fin structure, source region, and drain region of the first area to

be doped with phosphorus and causes the second fin structure, source region, and drain region of the second area to be doped with boron, as required by claim 1.

For at least the foregoing reasons, Applicants submit that claim 1 is patentable over WU et al. and FRENETTE et al., whether taken alone or in any reasonable combination.

Claims 2-6 depend from claim 1. Therefore, these claims are patentable over WU et al. and FRENETTE et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1.

Independent claim 7 recites features similar to features recited above with respect to claim 1. Therefore, claim 7 is patentable over WU et al. and FRENETTE et al., whether taken alone or in any reasonable combination, for reasons similar to reasons given above with respect to claim 1.

Claims 8-12 depend from claim 7. Therefore, these claims are patentable over WU et al. and FRENETTE et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 7.

Claims 15-19 depend from claim 13. The disclosure of FRENETTE et al. does not remedy the deficiencies in the disclosure of WU et al. set forth above with respect to claim 13. Therefore, claims 15-19 are patentable over WU et al. and FRENETTE et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 13.

New claim 20 depends from claim 13. Therefore, this claim is not anticipated by WU et al. for at least the reasons given above with respect to claim 13. Moreover, this claim recites additional features not disclosed or suggested by WU et al.

Claim 20 recites that the forming a first glass layer includes forming the first glass layer directly on the fin structures of the first area and the second area. In stark contrast, WU et al. discloses the first glass layer being formed on gate structure 8 (see, for example, Figs. 7A and 8A) and not, as required by claim 20, directly on the fin structure.

In view of the foregoing amendment and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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